WHAT IS CLAIMED IS:

1. An apparatus, comprising:

a comparator to receive an analog input signal V_{IN} along with a comparison signal V_C and to generate a digital result; and

an adjustment circuit to adjust the comparison signal based on successive digital results from the comparator.

2. The apparatus of claim 1, wherein the adjustment circuit includes:

an higher-threshold portion associated with a higher-threshold signal V_H; and

a lower-threshold portion associated with a lower-threshold signal V_L, wherein V_C substantially equals $(V_H + V_L)/2$.

3. The apparatus of claim 2, wherein the comparator receives V_C from a comparison node and:

the higher-threshold portion of the adjustment circuit includes:

a higher-threshold sample and hold element to receive V_C and to selectively provide V_H to an higher-threshold node, and

a higher-threshold resistor having a resistance R coupled between the higher-threshold node and the comparison node; and

the lower-threshold portion of the adjustment circuit includes:

a lower-threshold sample and hold element to receive V_C and to selectively provide V_L to a lower-threshold node, and

a lower-threshold resistor having a resistance substantially equal to R and being coupled between the lower-threshold node and the comparison node.

4. The apparatus of claim 3, wherein the higher-threshold and lower-threshold sample and hold elements are amplifiers each having an output that is isolated from an input.

5. The apparatus of claim 3, further comprising:

a first switch coupled between the higher-threshold node and a reference voltage; and

a second switch coupled between the lower-threshold node and ground.

6. The apparatus of claim 5, wherein the first and second switches are to be closed to initialize V_H to the reference voltage and V_L to ground.

7. The apparatus of claim 5, further comprising:

a third switch coupled between the output of the higher-threshold sample and hold element and the higher-threshold node; and

a fourth switch coupled between the output of the lower-threshold sample and hold element and the lower-threshold node.

8. The apparatus of claim 1, further comprising:

a multi-bit result register to store results from the comparator.

9. The apparatus of claim 1, wherein the adjustment circuit is further to convert multiple digital input signals into an analog output signal V_{OUT}.

10. A method, comprising:

comparing an analog input signal V_{IN} to a comparison signal V_C;

providing a digital result of the comparison;

adjusting V_C based on the digital result; and

successively performing comparisons, stores, and adjustments to generate a digital representation of V_{IN}.

11. The method of claim 10, wherein said adjusting includes:

initially setting a higher-threshold signal V_H; and

initially setting a lower-threshold signal V_L, wherein V_C substantially equals $(V_H + V_L)/2$.

12. The method of claim 11, further comprising:

when a digital result indicates V_{IN} is less than the existing V_C, setting V_H to the existing V_C.

13. The method of claim 12, wherein V_H is set to the existing V_C by transferring the existing V_C through a sample and hold element.

14. The method of claim 11, further comprising:

when a digital result indicates V_{IN} is not less than the existing V_C, setting V_L to the existing V_C.

15. The method of claim 15, wherein V_L is set to the existing V_C by transferring the existing V_C through a sample and hold element.

16. The method of claim 11, wherein V_H is initially set to a reference voltage and V_L is initially set to ground.

17. The method of claim 10, wherein said providing comprising:

storing results in a multi-bit result register.

18. A system, comprising:

a processor having an analog to digital conversion portion that includes:

a comparator to receive an analog input signal V_I along with a comparison signal V_C and to generate a digital result, and

an adjustment circuit to adjust the comparison signal based on successive digital results from the comparator; and

a battery input to receive power to be provided to the processor.

19. The system of claim 18, wherein the adjustment circuit includes:

an higher-threshold portion associated with a higher-threshold signal V_H; and

a lower-threshold portion associated with a lower-threshold signal V_L, wherein V_C substantially equals $(V_H + V_L)/2$.

20. The system of claim 19, wherein the comparator receives V_C from a comparison node and:

the higher-threshold portion of the adjustment circuit includes:

a higher-threshold sample and hold element to receive V_C and to selectively provide V_H to an higher-threshold node, and

a higher-threshold resistor having a resistance R coupled between the higher-threshold node and the comparison node; and

the lower-threshold portion of the adjustment circuit includes:

a lower-threshold sample and hold element to receive V_C and to selectively provide V_L to a lower-threshold node, and

a lower-threshold resistor having a resistance substantially equal to R and being coupled between the lower-threshold node and the comparison node.